ABSTRACT OF THE DISCLOSURE

A method of cell placement and clock tree synthesis includes steps of: (a) identifying critical paths in an integrated circuit design; (b) partitioning the integrated circuit design into a timing group for each of the critical paths; (c) assigning each flip-flop in a critical path to a timing group corresponding to the critical path; (d) performing a cell placement to minimize a function of propagation delay and maximum distance between flip-flops within each timing group; and (e) constructing a clock sub-net for each timing group.